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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/788,216	02/16/2001	Hanan Potash	5625-00300	3918

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EXAMINER	
KADING, JOSHUA A	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/788,216	POTASH, HANAN	
	Examiner	Art Unit	
	Joshua Kading	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8,12-19,21,22,25 and 29* is/are rejected.

7)☒ Claim(s) *5, 7, 9-11, 20, 23, 24, and 26-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 February 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 6, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, applicant states "may contain..." This is vague and does not properly define applicant's invention. By placing the word "may" in the claim, applicant has essentially given no weight to the limitations of claim 2. If something may (or may not) be part of applicant's invention, what importance can it possibly have? It must be assumed, since applicant's invention gives no importance to whether or not the interface has the scrambler or not, that applicant is trying to claim all possible scenarios in which an interface can or cannot have a scrambler, thus making the claim's metes and bounds impossible to distinguish.

Regarding claims 2 and 15, it is unclear from the claims and the specification how applicant defines scrambler/de-scrambler. For example, in Muhammad et al. (U.S. Patent 6,650,649 B1) scrambler is defined as an energy dispersion device (col. 28, lines 35-36), however, Saeki et al. (U.S. Patent 4,322,745) defines a scrambler as a device for "mixing up" a signal so that others cannot eavesdrop on a transmission (Abstract,

lines 1-7). Applicant is reminded that undefined terms or terms with more than one meaning must be clearly defined in the specification. See MPEP 2106.II.C section on applicant acting as own lexicographer.

Applicant states, in claim 6, that the first queue manager has a first capture queue that transfers data from the computer processor to the transmitted frame, and the second queue manager has a second capture queue that removes data from the received frame. Claim 1 however, states that the first queue manager removes the data from the received frame and that the second queue manager transfers queued data to the transmitted data stream. Therefore, it is unclear what applicant regards as the invention. Is it what is described in claim 1 or in claim 6, as they seem to contradict each other?

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 8, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (U.S. Patent 5,619,497) in view of applicant's admitted prior art (AAPA).

Regarding claim 1, Gallagher discloses "a communications interface between an...network and a computer processor or a communication switch (figure 12 shows a switch network 10 connected to processor element 306), said interface is adapted to synchronously receive and transmit a serial data stream (figure 14, elements 341 and 342 which are part of the shared node of figure 12), said communications interface (it should be noted that although some portions of the interface are described with respect to figure 3 and its components, figures 12-14A use the same components as in figure 3 and as such the referenced columns and lines are used to describe both figure 3 and figures 12-14A) comprising:

a first queue manager segment adapted to remove a first portion of the data from a frame of the received data stream and transfer the removed data to the computer processor (col. 7, lines 34-45 where Frame receiver 110 acts as the queue manager for the header portion (the first portion) of the frame (as well as the data portion) by separating the header from the frame and placing it in the appropriate queue ready to be sent to processor 120);

a second queue manager segment adapted to transfer data from the computer processor into a frame of the transmitted data stream (figure 3, element 140 act as the second queue manager by transferring data from the computer processor to a transmitting data stream as described in col. 8, lines 9-18; further the data from the computer processor is the header as indicated by the data path from the processor 120 to element 140);

a pass-through buffer segment that transfers a second portion of the received frame to the transmitted frame, absent transferring the received frame to the computer processor (figure 3, element 164 acts as a buffer segment for the second portion (data) from the local memory ready to be transmitted as read in col. 8, lines 30-37);

a first frame index adapted to compute a unique physical address within the received frame of a byte in the received data stream (col. 10, lines 61-col. 11, lines 1-8 where the sequence field comes from the frame header and represents the first frame index, and when the data is stored in the table the sequence field corresponds to a physical address used to store the data);

a second frame index adapted to compute a unique physical address within the transmitted frame of a byte in the transmitted data stream (col. 24, lines 28-40 where the D_ID is a acts as the second frame index used to compute the physical address (or port address) of the transmitted data);

first pointer control logic adapted to maintain a pointer to a payload portion of the received frame (col. 9, lines 6-9 where the previous data pointer register is the control logic);

second pointer control logic adapted to maintain a pointer to a payload portion of the transmitted frame (col. 9, lines 9-13 where the current data pointer register is the second pointer control logic);

a first index adapted to compute a unique logical address for a byte within the payload portion of the received frame (col. 21, lines 59-67 where the tag acts as a first

index used to compute the logical address or contents of the cache currently loaded); and

a second index adapted to compute a unique logical address for a byte within the payload portion of the transmitted frame (col. 21, lines 59-67, although col. 21 describes the Receive Frame Manager, it is stated in col. 8, lines 30-37 that the Receive and Transmit Frame Managers function similarly, thus the Transmit Frame Manager will generate a second index or tag for computing a logical address for the transmitted portion)."

However, Gallagher lacks what AAPA discloses, that the network is an optical network (Specification, page 1, lines 10-20 where AAPA makes reference to the connection between a Fibre Channel network such as in Gallagher and the SONET network described in AAPA).

It would have been obvious to one with ordinary skill in the art at the time of invention to have the network consist of an optical network for the purpose of increasing the bandwidth of the system. The motivation for increasing bandwidth of a network is to allow for more data (that could be more users and/or larger amounts of data per user) to be communicated over the network.

Regarding claim 3, Gallagher and AAPA disclose the interface of claim 1. However, AAPA lacks what Gallagher further discloses, "the first pointer control logic further comprises a table containing an offset to the start of one or more payloads within the received frame (figure 1, element 178 represents a "context" or table, i.e. a series of

registers, that contain the offsets (the pointers) to the payload sections as read in col. 9, lines 6-13), and the second pointer control logic further comprises a table containing an offset to the start of one or more payloads within the transmitted frame (figure 1, element 178 represents a "context" or table, i.e. a series of registers, that contain the offsets (the pointers) to the payload sections as read in col. 9, lines 6-13 and although element 178 refers to receiving device, col. 8, lines 30-37 state the transmitting device is similar in nature to the receiving device)." It would have been obvious to one with ordinary skill in the art to include the pointer logic with tables for the same reasons and motivation as in claim 1.

Regarding claim 8, Gallagher and AAPA disclose the interface of claim 1. However, Gallagher lacks what AAPA further discloses, "the transmitted and received frames comprise frames transmitted from or forwarded to a synchronous optical network (SONET) having different transfer rates (Specification, page 2, lines 16-27 where the "OC-n" indicates different transfer rates within the network)." It would have been obvious to one with ordinary skill in the art to have the optical network consist of a SONET network for the same reasons and motivation as in claim 1.

Regarding claim 12, Gallagher and AAPA disclose the interface of claim 1. However, AAPA lacks what Gallagher further discloses, "the interface is implemented as an integrated circuit (Abstract, lines 6-9)." It would have been obvious to one with

ordinary skill in the art to have the interface implemented as an IC for the same reasons and motivation as in claim 1.

Claims 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (U.S. Patent 5,619,497).

Regarding claim 4, Gallagher discloses the interface of claim 3. However, Gallagher explicitly lacks "the table of the first control logic and the table of the second control logic each comprise a two-port random access memory." Although Gallagher does not disclose what type of memory device is used to store the tables of the first and second control logic, applicant indicates that this is a matter of design choice (see specification, page 7, lines 2-3) where the table MAY be implemented by a two-port random access memory, thus leaving open the possibility for other forms of memory such as the type used in Gallagher. It would have been obvious to one with ordinary skill in the art at the time of invention to include a memory device of a designers choosing for the purpose of storing the frames of consecutively received packets to be processed soon thereafter (Gallagher, col. 2, lines 24-36). The motivation for storing the frames of the packets is so that no packets are lost or transmitted out of order.

It is believed applicant intends to claim the invention as described in independent claim 1, therefore it is assumed that the functions of the first queue manager and second queue manager (and thusly the capture queues) are as described in claim 1.

Regarding claim 6, Gallagher discloses the interface of claim 1. However Gallagher explicitly lacks that "each of the first and second queue managers contains an overhead capture queue..." Although Gallagher does not explicitly state that the queues are in the queue managers, he does disclose the first queue to be outside the queue manager (figure 3, element 114) and the second queue is implied to be in the second queue manager (col. 8, lines 12-18 whereby having the data in a queue ready for transmission suggests that the headers of the respective data frames must also be waiting in a queue (or buffer) of some kind to be matched with their appropriate data frame). Further, Gallagher discloses that these queues "the overhead capture queue of the [second] queue manager is adapted to transfer data from the computer processor into the manifest portion of the transmitted frame (col. 8, lines 12-18), and the overhead capture queue of the [first] queue manager is adapted to remove data from the manifest portion of the received frame and transfer it to the computer processor (col. 7, lines 37-41)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the queues in the queue managers as a matter of design choice, further the queue of the receiving manager is a necessary part of the receiving portion because the headers that are removed must be stored in a location prior to being processed (Gallagher, col. 2, lines 24-36). The motivation for having the queues in the queue managers would be to allow for less delay in transferring data from one piece of hardware to another, i.e. having memory on the same "chip" as a processor means faster storing and fetching of data from the memory than if it were outside the processor "chip", as is known in the art.

Since the word "may" renders claim 2 vague and indefinite, claim 2 will be treated as if the word "may" were not there. Further, since applicant is unclear how scrambler/de-scrambler is defined, Saeki will be used as the assumed definition.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. in view of Saeki et al. (U.S. Patent 4,322,745 B1).

Regarding claim 2, Gallagher discloses the interface of claim 1. However, Gallagher lacks what Saeki discloses, the interface "contain[s] one or more scrambler/de-scramblers adapted to operate in byte-parallel mode (figure 2, elements 32, 33, and 34 and figure 3, elements 41, 42, and 43 and are operating in byte-parallel mode)." It would have been obvious to one with ordinary skill in the art at the time of invention to have the signals scrambled for the purpose of preventing others from eavesdropping. The motivation for the prevention of eavesdropping is so that the information being transmitted may not be stolen or taken illegally (Saeki, abstract, lines 1-7).

Claims 13, 14, 16, 17, 18, 19, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. in view of Trbovich et al. (U.S. Patent 4,965,804) and in further view of applicant's admitted prior art (AAPA).

Regarding claim 13, Gallagher discloses "a method for interfacing a...communications network to a computer processor, comprising:

synchronously receiving a frame of serialized data from the network as an incoming data stream (figure 14, element 342 which is part of the shared node of figure 12 and receives serial data at element 342);

removing at least some of the data from the received frame and transferring the removed data to the computer processor (col. 7, lines 34-45 where Frame receiver 110 acts removes the header data of the frame (as well as the data portion) by separating the header from the frame and placing it in the appropriate queue ready to be sent to processor 120);

transferring data from the computer processor to a transmitted frame (col. 8, lines 9-18 where the data from the processor 120 is sent to the Transmit Frame Manager 140 and then placed in the transmitted frame)..."

However, Gallagher lacks what Trbovich discloses, "sending the transmitted frame as an outgoing data stream, such that the first byte of the outgoing data stream is adapted to be sent before the last byte of the incoming data stream has been received (col. 6, lines 37-44)."

It would have been obvious to one with ordinary skill in the art at the time of invention to have the first byte being transmitted before the last byte has been received for the purpose of having a low delay on packet transmissions. The motivation for a low delay is faster receipt after initial transmission of data, thus making the network appear faster.

Gallagher and Trbovich, however, further lack what AAPA discloses, that the network is an optical network (Specification, page 1, lines 10-20 where AAPA makes

reference to the connection between a Fibre Channel network such as in Gallagher and the SONET network described in AAPA).

It would have been obvious to one with ordinary skill in the art at the time of invention to have the network consist of an optical network for the purpose of increasing the bandwidth of the system. The motivation for increasing bandwidth of a network is to allow for more data (that could be more users and/or larger amounts of data per user) to be communicated over the network.

Regarding claim 14, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "queuing the incoming data stream in an input capture queue (figure 14, elements 350 represent queues of the incoming data), and queuing the outgoing data stream in an output capture queue (figure 14, elements 354 are the outgoing queues of the data)." It would have been obvious to one with ordinary skill in the art to have the input and output queues with the method of claim 13 for the same reasons and motivation as in claim 13.

Regarding claim 16, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "using first and second tables to record the offset to the start of one or more payload portions in the received and transmitted frames, respectively (figure 14A, elements 386 and 392 as described in col. 8, lines 30-37 and 47-57 where elements 100 and 140 are the same as elements 386 and 392, further the "context" 178 is the functional equivalent of a table

because the way in which it stores and accesses the data, including pointers to more permanently stored data)." It would have been obvious to one with ordinary skill in the art to have the tables for storing offsets for the same reasons and motivation as in claim 13.

Regarding claim 17, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "using a frame index to record the physical address with respect to the received frame of a byte within the incoming serial data stream (col. 10, lines 61-col. 11, lines 1-8 where the sequence field represents the frame index, and when the data is stored in the table the sequence field corresponds to a physical address used to store the data)." It would have been obvious to one with ordinary skill in the art to have the frame index for recording a physical address of stored data for the same reasons and motivation as in claim 13.

Regarding claim 18, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "using an index to record the logical address with respect to the payload portion of the received frame of a byte within the incoming byte data stream (col. 21, lines 59-67 where the tag acts as an index used to record the logical address of the payload associated with the cache)." It would have been obvious to one with ordinary skill in the art to the index for recording the logical address of the payload portion of the data for the same reasons and motivation as in claim 13.

Regarding claim 19, Gallagher, Trbovich, and AAPA disclose the method of claim 16. However, Gallagher, Trbovich and AAPA explicitly lack "implementing the first and second tables as two-port random access memory devices." Although Gallagher does not disclose what type of memory device is used to store the tables, applicant indicates that this is a matter of design choice (see specification, page 7, lines 2-3) where the table MAY be implemented by a two-port random access memory, thus leaving open the possibility for other forms of memory such as the type used in Gallagher. It would have been obvious to one with ordinary skill in the art at the time of invention to include a memory device of a designers choosing for the purpose of storing the frames of consecutively received packets to be processed soon thereafter (Gallagher, col. 2, lines 24-36). The motivation for storing the frames of the packets is so that no packets are lost or transmitted out of order.

Regarding claim 21, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "using a first overhead capture queue adapted to transfer data from the manifest portion of the received frame to the computer processor (figure 14, elements 352 store the header as read in col. 23, lines 38-43)." It would have been obvious to one with ordinary skill in the art to have a queue store the manifest (header) portion of the frame for the same reasons and motivation as in claim 13.

Regarding claim 22, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "using a second overhead capture queue adapted to transfer data from the computer processor to the manifest portion of the transmitted frame (col. 8, lines 12-18 whereby having the data in a queue ready for transmission suggests that the headers of the respective data frames must also be waiting in a queue (or buffer) of some kind to be matched with their appropriate data frame)." It would have been obvious to one with ordinary skill in the art to have the second capture queue for the same reasons and motivation as in claim 13.

Regarding claim 25, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Trbovich and AAPA lack what Gallagher further discloses, "a frame comprises a data structure adapted for transmission over a synchronous optical network (SONET) having differing transfer rates. (Specification, page 2, lines 16-27 where the "OC-n" indicates different transfer rates within the network)." It would have been obvious to one with ordinary skill in the art to have the optical network consist of a SONET network for the same reasons and motivation as in claim 13.

Since applicant is unclear how scrambler/de-scrambler is defined, Saeki will be used as the assumed definition.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al., Trbovich et al., and AAPA as applied to claim 13 above, and further in view of Saeki et al.

Regarding claim 15, Gallagher discloses the method of claim 13. However, Gallagher lacks what Saeki discloses, the interface "scrambling the incoming data and de-scrambling the outgoing data, using a scrambler/de-scrambler circuit adapted to operate in byte-parallel mode (figure 2, elements 32, 33, and 34 and figure 3, elements 41, 42, and 43 and are operating in byte-parallel mode)." It would have been obvious to one with ordinary skill in the art at the time of invention to have the signals scrambled for the purpose of preventing others from eavesdropping. The motivation for the prevention of eavesdropping is so that the information being transmitted may not be stolen or taken illegally (Saeki, abstract, lines 1-7).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al., Trbovich et al., and AAPA as applied to claim13 above, and further in view of Shobatake et al. (U.S. Patent 5,274,641).

Regarding claim 29, Gallagher, Trbovich, and AAPA disclose the method of claim 13. However, Gallagher, Trbovich, and AAPA lack what Shobatake discloses, "using a changeable "fill byte" to replace data removed from the received frame, before transferring the data to the transmitted frame (col. 13, lines 24-30 where the empty cell is the functional equivalent to the "fill byte" because they are both used to replace non-existent data in a transmitted packet)." It would have been obvious to one with ordinary skill in the art at the time of invention to include the empty cell for the purpose of synchronizing the output data stream. The motivation for synchronizing the output data

stream is so that it may be transmitted without error caused by a non-synchronized packet being sent.

Allowable Subject Matter

Claims 5, 7, 9-11, 20, 23, 24, and 26-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua Kading whose telephone number is (703) 305-0342. The examiner can normally be reached on M-F: 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas Olms can be reached on (703) 305-4703. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KENNETH VANDERPUYE
PRIMARY EXAMINER

Joshua Kading

Examiner
Art Unit 2661

August 4, 2004